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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/034,273	12/28/2001	David Chatenever	02580-P0006B	9457
24126 7590 07/17/2007 ST. ONGE STEWARD JOHNSTON & REENS, LLC 986 BEDFORD STREET STAMFORD, CT 06905-5619			EXAMINER HENN, TIMOTHY J	
			ART UNIT 2622	PAPER NUMBER
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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/034,273	CHATENEVER ET AL.	
	Examiner	Art Unit	
	Timothy J. Henn	2622	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 25 April 2007.
- 2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☐ Claim(s) _____ is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-4 and 6-32 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 28 December 2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Arguments

1. Applicant's arguments with respect to the claims have been considered but are moot in view of the new ground(s) of rejection.

Claim Objections

2. Claim 24 is objected to because of the following informalities: Claim 24 requires "software for selecting hardware", however claims 22 and 23 require software for configuring hardware. For the purposes of art rejection, claim 24 will be read as requiring software for "configuring" hardware to provide proper antecedent basis for the "said software" limitation. Appropriate correction is required.

Claim Rejections - 35 USC § 103

3. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.
4. Claims 1-4 and 6-32 rejected under 35 U.S.C. 103(a) as being unpatentable over Mochida et al. (US 2004/0141054) in view of Nakamura et al. (US 5,627,583).

[claim 1]

Regarding claim 1, Mochida discloses a video imaging system (Figure 1), comprising: a camera head for transmitting image data (Figure 1, Item 3; Paragraph 0136); a camera control unit receiving and processing the image data from the camera

head (Figure 1, Item 4; Paragraph 0136), the camera control unit having a detachable configurable component (Figure 1, Items 41-43; Paragraphs 0227-0239; Mochida discloses an expansion substrate which uses an FPGA to process image data), wherein the detachable configurable component is completely removable from the camera control unit such that a different detachable configurable component may be installed in the camera control unit (e.g. Paragraph 0028; "disconnected freely"; Paragraphs 0174-0177). Mochida further discloses that the detachable configurable component can be configured according to received information (e.g. Paragraphs 0235-0237), but does not explicitly disclose that the configuration information is stored on a storage device accessible by the camera control unit.

Nakamura discloses a similar video imaging system (Figure 2) including a camera head (Figure 2, Item 1), camera control unit (Figure 2, Item 3) and a reconfigurable processing component (Figure 2, Item 16). Nakamura further discloses that information stored on a storage device accessible to the camera control unit can be used to properly configure the reconfigurable processing component according to the type of camera head connected (e.g. c. 4, ll. 5-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the reconfigurable processing components of Mochida in accordance with data stored on a storage device accessible to the camera control unit as taught by Nakamura to perform optimum processing on image data produced by the connected camera head (c. 4, ll. 52-57).

[claim 2]

Regarding claim 2, Nakamura further discloses that a camera head identifier can be sent to the camera control unit for retrieving the information from the storage device (Figure 6; c. 7, ll. 7-51).

[claim 3]

Regarding claim 3, Nakamura discloses a camera head which transmits the camera head identifier (Figure 6, Item 51, 52; c. 7, ll. 21-34; the examiner notes that since the camera head identifying means is located on the camera head, information must be "transmitted" as claimed to the camera control unit in some manner to inform the camera control unit of the identifier of the connected camera head).

[claim 4]

Regarding claim 4, Nakamura discloses a camera head which includes the storage device (Figure 2, Items 19, 20).

[claim 6]

Regarding claim 6, Nakamura discloses information for programming aa FPGA to optimally process image data (c. 4, ll. 5-57). The examiner notes that, as broadly as claimed, this information can be said to "specify" the at least one replaceable hardware component (e.g. the information provides a specification for the FPGA by which the image information is processed).

[claim 7]

Regarding claim 7, Mochida discloses a replaceable hardware component which further includes a processor (e.g. Figure 28, Item 452).

[claim 8]

Regarding claim 8, Mochida discloses a replaceable hardware component which further includes a memory device (Figure 28, Item 73).

[claim 9]

Regarding claim 9, Mochida discloses a replaceable hardware component which further includes a field programmable gate array (i.e. FPGA, Figure 28, Item 452; Paragraph 0229).

[claim 10]

Regarding claim 10, Mochida discloses a video bus and the replaceable hardware component attached to the video bus (Figure 1).

[claim 11]

Regarding claim 11, Mochida discloses a replaceable hardware component which includes a connector (Figure 2, Item 35; Paragraph 0145).

[claim 12]

Regarding claim 12, Mochida discloses a connector which receives image data (Paragraphs 0146-0147).

[claim 13]

Regarding claim 13, Mochida discloses a connector which outputs a signal processed from the image data (e.g. Paragraph 0143 discloses outputting to a monitor through D/A convert 36 and encoder 37 while Figure 23 and Paragraphs 0204-0226 disclose enlarging an image using the expansion substrates to display an enlarged image on the monitor, therefore the connect must include an output as claimed to output

processed image data).

[claim 14]

Regarding claim 14, Mochida discloses a camera control unit which further comprises hardware capable of processing at least two different types of image data (e.g. Paragraph 0194; image data from CCD sensors of varying sizes can be considered different "types" of image data).

[claim 15]

Regarding claim 15, Mochida discloses information which routes the image data received by the camera control unit to the hardware capable of processing specified type of image data (i.e. by programming the FPGA using the information, the image data is "routed" to a proper section of the FPGA which is capable of providing proper processing).

[claim 16]

Regarding claim 16, Nakamura discloses configuring a reconfigurable hardware component so that the camera control unit is capable of issuing commands to the camera head as claimed (c. 4, ll. 5-57).

[claim 17]

Regarding claim 17, Mochida discloses a video imaging system (Figure 1), comprising: a camera head for transmitting image data (Figure 1, Item 3; Paragraph 0136); a camera control unit receiving and processing the image data from the camera head (Figure 1, Item 4; Paragraph 0136), the camera control unit having a detachable configurable component (Figure 1, Items 41-43; Paragraphs 0227-0239; Mochida

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discloses an expansion substrate which uses an FPGA to process image data), wherein the detachable configurable component is completely removable from the camera control unit such that a different detachable configurable component may be installed in the camera control unit (e.g. Paragraph 0028; "disconnected freely"; Paragraphs 0174-0177). Mochida further discloses that the detachable configurable component can be configured according to received information (e.g. Paragraphs 0235-0237), but does not explicitly disclose that the camera control unit receives the information and configures the component as claimed.

Nakamura discloses a similar video imaging system (Figure 2) including a camera head (Figure 2, Item 1), camera control unit (Figure 2, Item 3) and a reconfigurable processing component (Figure 2, Item 16). Nakamura further discloses that information received by the camera control unit can be used to configure a reconfigurable processing component (e.g. c. 4, ll. 5-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the reconfigurable processing components of Mochida in accordance with data stored on a storage device accessible to the camera control unit as taught by Nakamura to perform optimum processing on image data produced by the connected camera head (c. 4, ll. 52-57).

[claim 18]

Regarding claim 18, Nakamura discloses a storage device accessible by the camera control unit (Figure 2, Items 19, 20).

[claim 19]

Regarding claim 19, Nakamura discloses information stored on the storage device (c. 4, ll. 5-57).

[claim 20]

Regarding claim 20, Mochida discloses a connector for outputting a signal processed from the image data (e.g. Figure 1, output of Item 37).

[claim 21]

Regarding claim 21, Mochida discloses a camera control unit which further comprises hardware capable of processing at least two different types of image data (e.g. Paragraph 0194; image data from CCD sensors of varying sizes can be considered different "types" of image data).

[claim 22]

Regarding claim 22, Mochida discloses a video imaging system (Figure 1), comprising: a camera head for transmitting image data (Figure 1, Item 3; Paragraph 0136); a camera control unit receiving and processing the image data from the camera head (Figure 1, Item 4; Paragraph 0136), the camera control unit having a detachable configurable component (Figure 1, Items 41-43; Paragraphs 0227-0239; Mochida discloses an expansion substrate which uses an FPGA to process image data), wherein the detachable configurable component is completely removable from the camera control unit such that a different detachable configurable component may be installed in the camera control unit (e.g. Paragraph 0028; "disconnected freely"; Paragraphs 0174-0177). Mochida further discloses a CPU to program the detachable configurable

component (Paragraph 0229), but does not explicitly disclose software executing on the camera control unit for configuring the detachable configurable component.

Nakamura discloses a similar video imaging system (Figure 2) including a camera head (Figure 2, Item 1), camera control unit (Figure 2, Item 3) and a reconfigurable processing component (Figure 2, Item 16). Nakamura further discloses that circuit data can be loaded into an FPGA to form a processing circuit (e.g. c. 4, ll. 5-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the reconfigurable processing components of Mochida in accordance with data stored on a storage device accessible to the camera control unit as taught by Nakamura to perform optimum processing on image data produced by the connected camera head (c. 4, ll. 52-57). The examiner notes that the "circuit data" of Nakamura can be read as "software executing on the camera control unit" (i.e. software executed by the CPU) since the circuit data controls the CPU to properly program the FPGA device.

[claim 23]

Regarding claim 23, Nakamura discloses a storage device accessible by the camera control unit (Figure 2, Items 19, 20).

[claim 24]

Regarding claim 24, Nakamura discloses software for configuring hardware which is stored on the storage device (c. 4, ll. 5-57).

[claim 25]

Regarding claim 25, Mochida discloses a method for video imaging, comprising the steps of: providing a camera for transmitting image data (Figure 1, Item 3; Paragraph 0136); providing a camera control unit for processing the transmitted image data (Figure 1, Item 4; Paragraph 0136); receiving information and configurable a detachable configurable component in the camera control unit to process the image data (Paragraphs 0227-0239). However, Mochida does not disclose coupling a storage device to a camera control unit, storing information on the storage device, retrieving the information from the storage device and executing the information on the camera control unit as claimed.

Nakamura discloses a similar video imaging system (Figure 2) including a camera head (Figure 2, Item 1), camera control unit (Figure 2, Item 3) and a reconfigurable processing component (Figure 2, Item 16). Nakamura further coupling the camera head including a storage device in which circuit data is stored to the camera control unit, retrieving the information and executing the information (i.e. programming the FPGA) in order to properly configure a reconfigurable hardware component to process image data (e.g. c. 4, ll. 5-57). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to configure the reconfigurable processing components of Mochida in accordance with data stored on a storage device accessible to the camera control unit as taught by Nakamura to perform optimum processing on image data produced by the connected camera head (c. 4, ll. 52-57). The examiner further notes that Mochida further discloses that the camera control unit can be reconfigured (i.e. removing a detachable configurable component

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and inserting a new detachable configurable component) in order to provide expandability (e.g. Paragraphs 0013-0029). It would be obvious to one of ordinary skill in the art following the teachings of Nakamura to retrieve the information from the storage device a second time and to configure the different detachable configurable component in the camera control unit in order to ensure that the newly attached configurable component is configured in such a way as to optimally processing image data (c. 4, ll. 5-57).

[claim 26]

Regarding claim 26, Mochida discloses coupling at least one replaceable hardware component to the camera control unit (e.g. Figure 1, Items 41-43; Paragraphs 0227-0239).

[claim 27]

Regarding claim 27, Mochida and Nakamura disclose configuring the replaceable hardware component (e.g. Mochida, Paragraphs 0227-0239; Nakamura, c. 4, ll. 5-57).

[claim 28]

Regarding claim 28, Mochida discloses processing at least two different types of image data (e.g. Paragraph 0194; image data from CCD sensors of varying sizes can be considered different "types" of image data).

[claim 29]

Regarding claim 29, Mochida discloses a detachable configurable component which comprises a processor (Figure 28, Item 452).

[claim 30]

Regarding claim 30, Mochida in view of Nakamura discloses a processor which receives and executes a program (i.e. circuit data; Nakamura, c. 4, ll. 5-57).

[claim 31]

Regarding claim 31, Mochida discloses a detachable configurable component which comprises a processor (Figure 28, Item 452).

[claim 32]

Regarding claim 32, Mochida in view of Nakamura discloses a processor which receives and executes a program (i.e. circuit data; Nakamura, c. 4, ll. 5-57).

Conclusion

5. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).


A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Timothy J. Henn whose telephone number is (571) 272-7310. The examiner can normally be reached on M-F 11-7.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lin Ye can be reached on (571) 272-7372. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

TJH
7/3/2007



LIN YE
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